WHAT IS CLAIMED IS:

1. A processor comprising:

a wakeup loop to hold scheduler instructions including unexecuted instructions, and to indicate ready instructions of the unexecuted instructions that may be ready to be executed;

at least one of the unexecuted instructions to wakeup and notify at least another of the unexecuted instructions to speculatively wakeup; and

a select loop to select at least one of the ready instructions for execution.

2. The processor of Claim 1 further comprising a collision handling technique.

3. The processor of Claim 2 wherein the collision handling technique includes a predict another wakeup technique.

4. The processor of Claim 3 wherein the predict another wakeup technique includes a PAW vector.

5. The processor of Claim 2 wherein the collision handling technique includes a scoreboard to indicate whether

dependent instructions of an executed instruction have executed.

6. The processor of Claim 5 wherein a pileup victims vector is computed based on the scoreboard.

7. The processor of Claim 1 wherein the scheduler instructions include executed instructions.

8. The processor of Claim 1 wherein the select loop generates a collision victim vector to identify collision victims.

9. The processor of Claim 8 wherein the collision victim vector is communicated to the wakeup loop.

10. The processor of Claim 1 wherein the wakeup loop includes;

a wakeup array to hold the scheduler instructions; and

wakeup logic to indicate the at least one of the unexecuted instructions that may be ready to be selected forexecution.

11. The processor of Claim 10 wherein the wakeup array includes;

a resource vector corresponding to each of the scheduler instructions to indicate dependencies upon resources; and

a PAW vector to indicate the resources needed by earlier instructions in the wakeup array.

12. The processor of Claim 10 wherein the wakeup logic is selected from the group consisting of AND/OR array logic, CAM-style logic, and RAM-style logic.

13. The processor of Claim 1 wherein the select loop includes select logic to generate a grant vector indicating at least one of the unexecuted instructions speculatively ready and granted execution.

14. The processor of Claim 1 wherein the wakeup loop is pipelined over at least two cycles.

15. A processor comprising:

a select-free scheduler including wakeup and select logic having a total execution latency, to schedule instructions for functional units that execute instructions

having an execution latency that is less than the total execution latency of the wakeup and select logic.

16. The processor of Claim 15 further comprising a dynamic instruction scheduler to execute instructions that have an execution latency that is at least equal to the total execution latency of the wakeup and select logic.

17. The processor of Claim 15 wherein the select-free scheduler includes;

a wakeup stage to hold scheduler instructions including unexecuted instructions, the wakeup stage including;

a wakeup array having resource vectors corresponding to the unexecuted instructions to indicate dependencies upon resources; and

wakeup logic to indicate at least one of the unexecuted instructions that may be ready to be selected for execution; and

select logic including speculative wakeup to indicate at least one of the unexecuted instructions that may be ready to be selected for execution.

18. The processor of Claim 17 further comprising a collision handling technique.

19. The processor of Claim 18 wherein the collision handling technique includes a predict another wakeup technique.

20. The processor of Claim 19 wherein the predict another wakeup technique includes a PAW vector.

21. The processor of Claim 18 wherein the collision handling technique includes a scoreboard to indicate whether dependent instructions of an executed instruction have executed.

22. The processor of Claim 21 wherein a pileup victims vector is computed based on the scoreboard.

23. A system comprising:

a random access memory device; and

a processor in communication with the random access memory device, the processor including;

a wakeup loop to hold scheduler instructions including unexecuted instructions, and to indicate ready instructions of the unexecuted instructions that may be ready to be executed;

at least one of the unexecuted instructions to wakeup and notify at least another of the unexecuted instructions to speculatively wakeup; and

a select loop to select at least one of the ready instructions for execution.

24. The system of Claim 23 including further comprising a collision handling technique.

25. The processor of Claim 24 wherein the collision handling technique includes a predict another wakeup technique.

26. The processor of Claim 25 wherein the predict another wakeup technique includes a PAW vector.

27. The processor of Claim 24 wherein the collision handling technique includes a scoreboard to indicate whether dependent instructions of an executed instruction have executed.

28. The processor of Claim 27 wherein a pileup victims vector is computed based on the scoreboard.

29. The processor of Claim 23 wherein the scheduler instructions include executed instructions.

30. The processor of Claim 23 wherein the select loop generates a collision victim vector to identify collision victims.

31. The processor of Claim 30 wherein the collision victim vector is communicated to the wakeup loop.

32. A method of issuing requesting instructions to an execution unit, comprising:

speculatively setting an indicator to indicate a requesting instruction is ready to be selected for execution;

during a cycle, selecting a predetermined number of the requesting instructions having a set indicator; and

resetting the indicator of the requesting instructions that are selected.

33. The method of Claim 32 wherein the predetermined number of selected instructions is one.

34. The method of Claim 32 further comprising handling collisions.

35. The method of Claim 34 wherein handling collisions includes generating a collision victims vector.

36. The method of Claim 34 wherein handling collisions includes generating a pileup victims vector.

37. The method of Claim 36 wherein generating a pileup victims vector includes reading a scoreboard and identifying pileup victims based upon the scoreboard.

38. The method of Claim 34 further comprising delaying setting the indicator based on predicting wakeup of another instruction.

39. A method of issuing unexecuted instructions to an execution unit, comprising:

generating resource vectors corresponding to the unexecuted instructions, the resource vectors including resource indicators to indicate availability of resources;

speculatively setting the resource indicators to indicate resources associated with corresponding ones of the unexecuted instructions are available so that the corresponding ones of the unexecuted instructions are ready to be executed; and

selecting a predetermined number of the corresponding ones of the unexecuted instructions.

40. The method of Claim 39 further comprising resetting the resource indicators corresponding to the unexecuted instructions that are selected.

41. The method of Claim 39 wherein the predetermined number of selected instructions is one.

42. The method of Claim 39 further comprising handling collisions.

43. The method of Claim 42 wherein handling collisions includes generating a collision victims vector.

44. The method of Claim 42 wherein handling collisions includes generating a pileup victims vector.

45. The method of Claim 44 wherein generating a pileup victims vector includes reading a scoreboard and identifying pileup victims based upon the scoreboard.

46. The method of Claim 42 further comprising delaying setting the resource indicators based on predicting wakeup of another instruction.